**Example of internship subject for M2 students**

**(this is not an internship offer, but it is a typical example of research subject proposed to M2 students)**

**Laboratory: TIMA**

**Supervisor:**

**Subject** : Built-In Self-Test solutions for high performance and reliable RF integrated circuits

## Context of the internship

Testing RF subsystems embedded in a complex SoC/SiP represents a challenging task. It can be said that RF testing inherits the difficulties of analog testing, but adding also the problem of handling high-frequency signals. The direct test and diagnosis of an RF device are based on the application of a high-frequency stimulus and the observation of its response. This usually requires the use of dedicated high-speed external test equipment and the provision of an adequate test access. However, the increase in operation frequency and the fact that RF blocks are currently embedded within a complete integrated system, turn these requirements quite difficult. Test access to internal nodes is usually impossible, and even in the case these nodes are reachable, there may be electrical losses in the transport of the signals between the chip and the external tester. The development of RF BIST solutions has a great potential to overcome these issues. Signal manipulations would remain internal, thus eliminating transport problems. However, the RF BIST road is not free of shortcomings either. The main one is usually the internal generation of adequate RF test stimuli to test the Receiver section. Only if we can devise strategies for simplifying or avoiding the generation of RF signals this approach can be successful.

Many different approaches for simplifying RF testing have been proposed in the literature for the last years. Thus, direct approaches such as the one proposed in [2] replicate traditional RF test equipment on a load board. The need of RF testers is eliminated and multiple test specifications can be extracted. However the design of the load board is too complex for its direct BIST implementation, limiting this approach to the test of discrete RF circuits.

Loop-back test and diagnosis of transceivers have also been widely explored [3–7] as a way to avoid the generation of RF test stimuli. The signal coming from the transmitter part of a transceiver is re-injected into the receiver facilitating a global test for the transceiver signal chain. The main advantage is that only baseband signals are

involved as well as that both the receiver and the transmitter are tested at once. Nevertheless, an on-chip implementation is not so simple since, in practice, some components need to be removed for testing [34] (namely the band-pass filter, close to the antenna, and the power amplifier in the transmission path), or a calibrated signal attenuator has to be introduced in the loopback connection to accommodate the PA output signal to the LNA input signal range [5].

Model-based test compaction strategies have been also proposed [8, 9]. These techniques aim to remove costly RF measurements from the test program by computing these performances from other easier-to-measure observables. This replacement is based on either analytical [8] or regression models [9]. Exploiting these models some costly measurements such as Error Vector Magnitude can be avoided, reducing this way test time and cost.

The use of simplified built-in test instruments has also been explored [5, 6, 10–17]. These test sensors are designed to translate RF performance parameters to a low-frequency signal (usually a DC level). Several test strategies have been presented that use integrated-peak detectors, root-mean-square sensors, power detectors, DC-probes, envelope detectors or process monitor circuits. However, each individual test sensor gathers limited information, so multiple test sensors and/or test configurations are needed to extract accurate performance figures.

## Objectives

There is not a widely accepted solution yet for incorporating BIST into integrated transceivers. The tasks in this internship are aimed to study the application and development of novel test solutions for RF circuitry that:

a) Minimize or eliminate added loads to the RF signal path. RF circuits, and specially mmW circuits, are extremely sensitive to loading effects. Built-in test sensors that tap into the RF signal path should be carefully co-designed to avoid performance degradation. In this line, non-intrusive solutions as the DLPM technique developed by the applicant [1], the Process Monitors presented in [16], or temperature sensors such as the ones presented in [18] are interesting research paths. □

b) Simplify or avoid the generation of RF tones. Dedicated RF tone generators based on RF VCOs, as the one presented in [12] offer a great RF performance, but at the cost of design complexity and a considerable area overhead. Simplifying test stimulus generators, reusing existing resources for up-conversion of baseband stimuli, or eliminating RF stimuli are research paths worth pursuing in this sense. □

c) Minimize the number of required measurements. Being able to accurately estimate the complete set of performances of an RF system while minimizing the number of required measurements is still an open issue. A cost-driven optimization of the set of RF measurements to filter redundant and costly measurements is also a promising path

for reducing RF test complexity and cost. □

## References


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